

IN THE CLAIMS:

Please note that all claims that remain pending and under consideration in the referenced application are shown below, in clean form, for clarity.

Please amend the claims as follows:

G¹ 31. (Three times amended) A semiconductor capacitor storage poly, comprising:
downwardly extending recesses; and
a plurality of contiguous mesas comprising a plurality of contiguous top surfaces forming a
maze-like structure.

32. The storage poly of claim 31, wherein said mesas extend in the X, Y and Z
coordinates.

G² 33. (Three times amended) A semiconductor capacitor storage poly, comprising:
downwardly extending recesses;
a plurality of contiguous webs comprising a plurality of contiguous top surfaces forming a maze-
like structure; and
hemispherical-grain polysilicon on at least some of said plurality of contiguous top surfaces.

34. (Amended) The storage poly of claim 33, wherein said webs extend in the X, Y
and Z coordinates.

35. (Twice amended) An intermediate semiconductor capacitor structure, comprising:
a storage poly structure with recesses formed therein;
a contiguous hemispherical-grain polysilicon layer over said storage poly structure; and
a mask over said hemispherical-grain polysilicon layer, said recesses being exposed through said
contiguous hemispherical-grain polysilicon layer and said mask.

37. (Previously amended) An intermediate semiconductor memory cell structure, comprising:
a storage poly structure;
low elevation regions of a hemispherical-grain polysilicon layer on said storage poly structure;
recesses formed in said storage poly structure and located laterally between said low elevation regions of said hemispherical-grain polysilicon layer; and
dielectric material at least lining the recesses.

38. (Previously amended) A semiconductor memory cell structure, comprising:
a storage poly structure;
regions of hemispherical-grain polysilicon on at least portions of an upper surface of said storage poly structure;
a plurality of recesses extending into said storage poly structure, at least some recesses of said plurality of recesses being located laterally between said regions of hemispherical-grain polysilicon; and
and a dielectric layer substantially coating an upper surface of said storage poly structure and substantially lining each of said plurality of recesses.

39. The semiconductor memory cell structure of claim 38, further comprising a cell poly structure over said dielectric layer.

G³ 40. (Twice amended) The semiconductor memory cell structure of claim 38, wherein said storage poly structure comprises a web-like structure comprising a plurality of contiguous top surfaces.

41. The semiconductor memory cell structure of claim 38, wherein at least some of said plurality of recesses extend into said storage poly structure.

42. (Previously amended) An intermediate semiconductor capacitor structure, comprising:
a storage poly structure;
a substantially confluent hemispherical-grain polysilicon layer on said storage poly structure; and
a mask positioned over said substantially confluent hemispherical-grain polysilicon layer, elevated portions of said hemispherical-grain polysilicon layer being exposed through said mask.

43. (Previously twice amended) An intermediate semiconductor capacitor structure, comprising:
a storage poly structure including recesses formed therein;
portions of a hemispherical-grain polysilicon layer substantially overlying upper portions of said storage poly structure; and
a mask positioned over said hemispherical-grain polysilicon layer, laterally between said recesses, and spaced apart from said storage poly structure by said hemispherical-grain polysilicon layer, said recesses in said storage poly structure being exposed through said mask.

44. (Previously amended three times) An intermediate semiconductor capacitor structure, comprising:
a storage poly structure with recesses formed therein;
a hemispherical-grain polysilicon layer on at least portions of the storage poly structure;
a mask overlying at least portions of said hemispherical-grain polysilicon layer located laterally between said recesses; and
dielectric material lining at least said recesses.

45. (Previously amended) An intermediate semiconductor memory cell structure, comprising:
a storage poly structure with recesses formed therein;
low elevation regions of a hemispherical-grain polysilicon layer on at least portions of the storage poly structure;
a mask overlying at least said low elevation regions of said hemispherical-grain polysilicon layer, said recesses being exposed between said low elevation regions of said hemispherical-grain polysilicon layer and through said mask; and
dielectric material at least lining said recesses.